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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,773	03/28/2001	Claude R. Gauthier	03226.064001	2630

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EXAMINER

MEHTA, ARUNKUMAR P

ART UNIT	PAPER NUMBER
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2128

6

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/819,773

Applicant(s)

GAUTHIER ET AL.

Examiner

Arunkumar P Mehta

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 28 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-4, 9-13, 15-19, 23 and 27-34 is/are rejected.
- 7) ☐ Claim(s) 5-8, 20-22, 24-26 and 35-37 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 03 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>28 July 2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This application has been examined.
2. Claims 1-37 have been examined.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: Page 7, paragraph 31, line 1 indicates schematic 52 which is not labeled on figure 3. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Interpretation

4. Claim 1 – The board model is interpreted as being a software model. The package model is being interpreted as being a software model of semiconductor devices. The chip model is being interpreted as being a software model of the chip.
5. Claim 4 – The Bump and Grid" is interpreted as "ball and Grid" also.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Herrell et al ("Modeling of Power Distribution Systems for High-Performance Microprocessors", IEEE, 1999), herein referred to as Herrell.

8. As per claim 14, Herrell teaches modeling a power converter, modeling a board, modeling a package, and modeling a chip model (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being obvious over Dennis J. Herrell et al ("Modeling of Power Distribution Systems for High-Performance Microprocessors", IEEE, 1999), herein referred to as Herrell in view of Hiroshi Shimamori (US 5,737,202), herein referred to as Shimamori.

11. As per claim 1 Herrell discloses a power converter model, a board model, a package model, and a chip model (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Herrell does not expressly disclose the plurality of the power converter models.

Shimamori discloses the plurality of the power converters (Fig 1, items 12, 13, and 23).

Shimamori does not teach implementation of the converters in a model. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with Shimamori to provide models of power converters.

12. As per claim 2 and 3 Herrell does not expressly disclose the plurality of DC to DC converter models and also four DC to DC converter models. Shimamori teaches a plurality of DC to DC converters (Fig. 1, item 12 and 13) and four DC to Dc converters (Fig. 5, items 56-59). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrel with Shimamori to provide models of power converters.

13. Claims 4, 9-13, 15-19, 23, and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell in view of Shimamori and further in view of Anderson.

14. As per claim 4 Herrell teaches the plurality of bump and grid models (Page 241, Section II 3rd paragraph), but it fails to teach the plurality of section models and plurality of channel models. Anderson et al (herein referred to as Anderson), US 6385565, teaches about the plurality of section models and the plurality of channel models (Fig. 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of

ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to get an accurate model.

15. As per claim 9 Herrell fails to teach the plurality of section models arranged in an interconnecting grid. Anderson teaches about section grids arranged in an interconnecting grid (Fig 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

16. As per claim 10 Herrell fails to teach the interconnecting grid is generally square shaped. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

17. As per claim 11 Herrell fails to teach the plurality of section models comprises nine section models. Anderson teaches the nine section models(Fig. 3A, column 8 lines 33-40). It is an 8x8 grid, which comprises 9 section models. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

18. As per claim 12 Herrell fails to teach the plurality of the section models are arranged in a three section by three section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

19. As per claim 13 Herrell to teach the plurality of channel models comprises ten section models. However, "Official Notice" has been taken by the examiner that any number of section models can be used to analyze a complex circuit for better and efficient simulation.

20. As per claim 15 Herrell discloses modeling a power converter, modeling a board, modeling a package, and modeling a chip (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Herrell does not expressly disclose modeling the plurality of the power converters.

Shimamori discloses the plurality of the power converters (Fig 1, items 12, 13, and 23).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with Shimamori to provide models of power converters.

21. As per claim 16 Herrell does not expressly disclose the plurality of power converters comprises four DC to DC power converters. Shimamori teaches the four DC to DC converters (Fig. 5, items 56-59). It would have been obvious to one of ordinary

skill in the art at the time of the invention was made to modify the teachings of Herrel with Shimamori to provide models of power converters.

22. As per claim 17 Herrell teaches about modeling a plurality of bump and grid components (Page 241, Section II 3rd paragraph), but it fails to teach modeling a plurality of chip sections and plurality of chip channels. Anderson teaches the chip section models and the chip channel models (Fig. 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to get an accurate model.

23. As per claim 18 Herrell fails to teach modeling a plurality of chip section forms generally a square shaped grid. Anderson teaches about chip grid is a square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

24. As per claim 19 Herrell fails to teach the generally square shaped grid comprises a three section by three section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

25. As per claim 23 Herrell in view of Shimamori and in further view of Anderson as applied to claim 4 teaches all the subject matter of claim 23.

26. As per claim 27 Herrell fails to teach the plurality of section models are arranged in an interconnecting grid. Anderson teaches about section grids arranged in an interconnecting grid (Fig 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

27. As per claim 28 Herrell fails to teach the interconnecting grid is square shaped. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

28. As per claim 29 Herrell fails to teach the plurality of section models comprises nine section models. Anderson teaches the nine section models (Fig. 3A, column 8 lines 33-40). It is an 8x8 grid, which comprises 9 section models. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

29. As per claim 30 Herrell fails to teach the plurality of the section models are arranged in a three section by three section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have

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been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

30. As per claim 31 Herrell in view of Shimamori and in further view of Anderson as applied to claim 23 teaches all the subject matter of claim 31.

31. As per claim 32, claim 32 is a method claim containing the same subject matter as the apparatus of claim 23. Claim 32 is rejected on the same basis as claim 23.

32. As per claim 33 Herrell fails to teach modeling a plurality of chip sections forms a generally square shaped grid. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

33. As per claim 34 Herrell fails to teach the generally square shaped grid is a three section by three section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

Allowable Subject Matter

34. Claims 5-8, 20-22, 24-26, and 35-37 are objected to as being dependent upon a rejected base claim (and assuming all other rejections are traversed), but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yip et al (US5,694,344) A method of electrically modeling a semiconductor package.

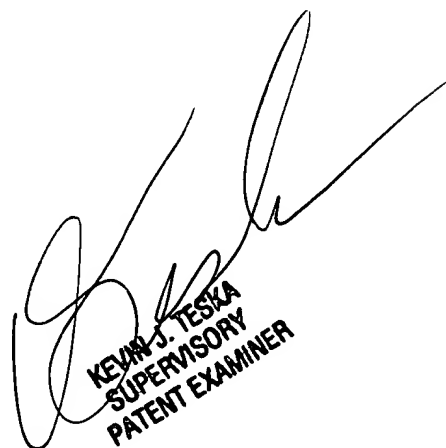
36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arunkumar P Mehta whose telephone number is 703-605-1227. The examiner can normally be reached on 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arunkumar P Mehta
Examiner
Art Unit 2128

APM



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